JITTER: SPECIFICATION AND ASSESSMENT IN DIGITAL AUDIO EQUIPMENT

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ABSTRACT

Timing jitter in digital audio equipment can subtley degrade the audio quality or even cause data transmission failure.

This paper examines the jitter performance requirements for digital audio equipment in the context of the audibility of sampling jitter modulation effects and the digital audio interface specification. It concludes by presenting techniques for the measurement of jitter performance.

1. INTRODUCTION

Digital audio signals are derived from sampling analogue audio signals at regular intervals. These sampling instants are at a constant rate - the sampling frequency. These signals are also re-sampled by asynchronous sampling frequency conversion and in digital to analogue convertors. The error in the sampling or re-timing instants is called sampling jitter. This jitter affects the quality of the final reproduced signal by adding potentially audible modulation sidebands to the original signal.

Often sampling jitter is confused with data link jitter. They are linked because inappropriate clock recovery circuits are often used for deriving sampling clocks from the interface signal - which will often have relatively high levels of jitter as a result of the information being carried. This data link jitter need not affect the quality of the finally reproduced signal - until it is so large that data errors are produced - and measurements of data link jitter may not give any clue as to sampling jitter in the associated equipment.

2. INTERFACE JITTER

The AES-3 digital audio interface for professional applications - defined in [1], (The EBU [2] and IEC-958 [4] versions are almost identical) and the similar consumer interface format, defined in IEC-958 and EIAJ CP-340 [3], define a bi-phase mark coded signal with an embedded clock.

There are two subframes of data per sample period (frame). Each subframe has 32 equal time slots. For slots 4 to 31 signal transitions always occur at time slot boundaries. There are also transitions at the centre of the time slot if the data bit carried in that time slot is a logic one. The preambles, in time slots 0 to 3, omit some of the time slot boundary transitions in order to flag the start of each data word. There are three types of preamble: X,Y and Z. X is used to identify the start of subframe 1, Y the start of subframe 2 and Z replaces every 192nd preamble X (to indicate a new channel status block).

2.1 Limitations of the AES-3 interface jitter specification

The AES-3 standard now provides a specification for the transmitter data link jitter. This is defined as follows:

6.2.5   Data Jitter

Data transitions shall occur within ±20 ns of an ideal jitter-free clock measured at the half-voltage points.

An ideal jitter-free clock may be defined as a clock signal at exactly twice the average time slot rate (or 128 times the average sampling frequency), with a phase adjusted against the signal such that the average timing error between any transition and the appropriate clock edge is zero.

Therefore it is necessary to be able to evaluate the phase and frequency of the signal before a measurement of the signal timing error can be made. The timescale over which these measurements are averaged needs to be defined. This could be over a finite period of time, but it would be much easier to measure continuously if the averages had decaying weightings over time. A phase locked loop, locked to every transition, would behave in this manner.

Including an averaging time into the jitter specification reduces the sensitivity of the specification to low frequency jitter. A low frequency limit would effectively be defined by the averaging time constant. Below this frequency equipment may track the phase variations of a received signal while higher frequency phase variations need to be attenuated.

2.2 Sources of transmitter jitter

Data link jitter can be produced by an interface transmitter. This is either as a result of the phase noise from an oscillator or from poor rejection of incoming jitter. The AES-3 specification, quoted above, applies to this jitter. The requirement to reject incoming jitter applies to transmitters that are synchronised to external sources - such as another AES-3 signal as defined in the synchronisation standard, AES-11 [5].

It is possible to produce wide frequency range RC multivibrator-based clock recovery circuits that have low enough phase noise for the AES-3 transmitter specification, at reasonable cost. Examples of this are in receiver integrated circuits produced by Crystal and Yamaha. These devices also reject incoming jitter at frequencies above the audio band. At lower jitter frequencies the recovered clock tracks the input jitter. If the incoming low frequency jitter already exceeds the 40 ns peak to peak range of the transmitter specification this will result in recovered clock jitter that also exceeds the transmitter specification. This can happen as a result of line induced jitter (described in section 2.3) without the previous transmitter being out of specification.

Clock recovery PLLs can also have peaks in their jitter transfer functions. If a design has a peak with gain $G(f_0)$ at frequency f_0, then a cascade of N similar designs will have an overall gain of $NG(f_0)$ at that frequency. This gain could result in signals exceeding the AES-3 specification, and following equipment may not be able to recover clock or data. This has been the reason for some combinations of equipment not working together - even though they may work with other equipment.

For these reasons it is important to specify and measure the jitter transfer function of any equipment claiming compatibility with AES-3.

2.3 Line induced jitter

Most digital audio links have a limited bandwidth. This attenuates the higher frequency components of the digital audio interface signal, and slows rise and fall times. A transition delay is introduced, and this varies depending on the data pattern in the previous time slots.

For a two level input signal composed of short and long pulses of $\pm V_{in}$ the pulse transition delay depends on the time taken for the output signal to cross zero after the input signal changes from $+V_{in}$ to $-V_{in}$.

A simple simulation model was used to approximate this effect, shown in figure 1. This has an exponential step response giving this result relating transition delay, t_d, link time constant, τ, and the pulse height attenuation:

$$e^{\frac{t_d}{\tau}} = 1 + \left|\frac{V_{out}(t_t)}{V_{in}}\right|$$

Where $V_{out}(t_t)$ is the output signal level at the time of the input data transition. This is dependent on the data pattern, and was simulated for a variety of patterns.

Figure 2 illustrates the phenomenon. For the 200 ns time constant the shorter pulses are attenuated. This produces a transition delay that is shorter than the delay after the longer pulses - which are less attenuated. This delay variation is jitter.

Also note how the output pulse amplitude depends on the widths of previous pulses. The extremes occur for maximum and minimum previous pulse amplitudes. As there are always transitions on the time slot boundaries the mid slot transitions always occur after a short pulse.

The simulation results show the longest delay (1), shortest delay (2) and maximum delay difference (3) for the slot boundary (fig 4), slot centre (fig 3) and penultimate Y-preamble (fig 4) transitions for different time constants at a sample rate of 48kHz. These show that for link time constants of up to 50ns the transition delays are independent of data pattern. At longer time constants there is an increasing difference, with the preamble unaffected until $\tau > 200$ns. For the mid slot transition the minimum delay starts to be reduced for $\tau > 120$ns. This delay reduces to zero for a pulse that only just crosses the zero point, and before that occurs the signal is recoverable.

Peak to peak jitter levels can be deduced from these worst case timing variations. Cell boundary and the penultimate Y preamble transition jitter have been plotted against the 3dB bandwidth ($1/2\pi\tau$) in figure 6. This shows peak to peak data link jitter measured at the data slot boundaries exceeding 10ns for bandwidths less than approximately 1.8MHz. The curve for preamble jitter shows less than 1ns of jitter for link bandwidths down to below 1 MHz.

These figures illustrate the magnitude of the jitter that can be induced in typical lines. Real transmission lines may have more complicated characteristics but these figures may be used to approximate the effect of link bandwidth on jitter at the different transitions in the data stream.

Non-linear interfaces, such as the optical variant of the consumer format, have asymmetric characteristics. This is illustrated later in the paper.

2.4 Interface jitter measurement

The most common method quoted for examination of jitter is to trigger an oscilloscope on the signal and measure the transition broadening after a delay. This is insensitive to jitter of period longer than the delay, and may explain the limitations of some of the available devices.

2.4.1 Interface jitter amplitude

Figure 7 illustrates a method of measuring the jitter of a signal without reference to its synchronisation source. A good AES-3 receiver is required to regenerate the frequency of the notional ideal jitter-free clock. The jitter transfer function of this latter device can be measured, and then that will define the lower frequency of jitter that this test can measure.

An oscilloscope can be used to view the interface waveform against a trigger derived from the regenerated clock. This can be the re-clocked waveform or a sample rate clock. The latter will allow jitter at various points in the waveform to be examined. As explained in the previous section jitter in the data area may be a predominantly a result of the transmission line high frequency losses. As line induced jitter does not significantly effect the preambles, the jitter viewed here is more likely to

indicate that the preceding transmitter is at fault. These two types of jitter have been called `data jitter' and `word clock jitter'.

It is rare for equipment to exceed the AES-3 transmitter jitter specification whilst free-running. More common is equipment that cannot lock to sources whose jitter is well within that specification (though that specification does not directly apply to receivers). This test can be used to confirm this latter point.

2.4.2 Interface jitter transfer function

Figure 8 shows the more complex method used to measure the jitter transfer function.

The digital signal source provides the reference clock and the source of AES-3 signal. The delay modulator allows sinusoidal jitter to be applied to the device under test (DUT). The oscilloscope can display the applied jitter or DUT output jitter against the reference clock (using switch SW2). This reference may be switched between the interface signal and the sample clock of the source.

This arrangement can also be used to measure the total jitter noise of a DUT. Mute the data from the signal source and remove the modulator from the chain so that a minimum of jitter is applied to the DUT. The clock from the source is now a perfect jitter-free clock with a fixed phase offset. This allows the operator to measure low frequency jitter noise produced by the DUT with a jitter free input.

Jitter transfer functions most commonly have unity gain up to the lower jitter attenuation frequency. At this point there may be a peak of a few dB, followed by attenuation increasing at 12 dB per octave. Measurements on available equipment have shown lower jitter attenuation frequencies as high as 150 kHz and as low as 0.5 Hz.

2.4.3 Response to line-induced jitter

The previous test can also be applied to a transmission line in front of the DUT. This allows assessment of the response to line-induced jitter. For best results the signal source should be producing a low level 24 bit undithered square wave of 0 and -1 LSB levels. This will induce jitter at the square wave frequency and its harmonics.

This test reveals the clock recovery method the DUT uses. If the clock is recovered from the preamble transitions then the DUT will be very insensitive to the line-induced jitter - except for very large time constants (see figure 4).

A measurement of this type was used on an expensive two box consumer CD player. A CD with a -60dBFS 16 Hz tone was used to provide the signal. Measurement of the recovered clock in the DAC half of the player showed that with this signal the jitter increased to 10 ns using the coaxial input through a bandwidth limiting transformer and about 5 ns on the optical input.

The fact that this effect is related to the signal indicates that the unit was extracting clock information from the data area of the waveform rather than from the preambles so the time slot boundary curve of figure 6 can be used. Referring to the figure, this indicates that the coaxial link bandwidth was lower than 2 MHz. While the optical interface bandwidth was approximately twice this. (This unit uses a crystal based PLL with a lower corner frequency of approximately 2 kHz.)

3. SAMPLING JITTER

Sampling jitter in equipment can be measured in two ways. Either by taking the equipment apart and comparing the timing signals with a derived (relatively) ideal clock, or by measuring the effect on the audio using a spectrum analyzer. The first approach may not be convenient - and could be impossible if the re-sampling is occurring within a digital filter in a sample rate convertor. The

second approach has the advantages that it allows the equipment to operate in the manner intended and it also provides more information about the spectrum of the jitter and the audibility of the errors.

3.1 Sources of sampling jitter

For ADC and DAC jitter the sources are similar to those mentioned in section 2.2.

For digital audio synchronizers and sample rate convertors the sampling jitter can be dominated by the time resolution of the oversampling filters. This may not always be quoted but can be discovered by similar measurements to those for other types of sampling jitter. A 2048 times oversampling filter used in a synchroniser will introduce 10 ns steps for a 48 kHz sample rate - comparable with 10ns peak to peak jitter.

3.2 The effects of sampling jitter

An earlier paper by Meitner and Gendron [6] defined a target specification. This was determined by calculating the amplitude of jitter that will produce an error of amplitude 1 LSB when driven by a signal of worst case slew rate - that is a maximum level 20 kHz tone. This gives a result of 250ps (500ps pk-pk) for the maximum allowable level of spectrally white jitter for a 16 bit signal. This derivation assumes that it is acceptable for jitter to raise the noise floor by no more than 3 dB and makes no allowance for the jitter spectrum.

Kloker, Wernimont and Liu, in describing the new Motorola digital audio transceiver device [7] have made Fourier transform analyses of the audio signal in order to assess susceptibility to jitter. Unfortunately they did not try the worst case of low level limited bandwidth signals as the synchronisation source. This may have revealed jitter susceptibility in the test arrangement they describe.

The effect of sampling jitter is to phase modulate the signal. The equation for this process on a signal tone, with jitter of frequency ω_j and peak to peak amplitude J is as follows:

$$v(t) = A \cos[\omega_i(t + \tfrac{1}{2}J \sin \omega_j t)]$$

Where v(t) is the resultant signal, A the signal amplitude, ω_i the input signal frequency.

This equation can be rearranged to:

$$v(t) = A \cos(\omega_i t) \cos(\tfrac{1}{2}J\omega_i \cos(\omega_j t)) - A \sin(\omega_i t) \sin(\tfrac{1}{2}J\omega_i \cos(\omega_j t))$$

Considering small modulation levels ($J\omega_i \ll 1$) this approximates to:

$$v(t) = A[\cos(\omega_i t) + \tfrac{1}{4}J\omega_i \sin((\omega_i - \omega_j)t) + \tfrac{1}{4}J\omega_i \sin((\omega_i + \omega_j)t)]$$

This is equivalent to the original tone or `carrier' with sidebands at a spacing equivalent to the jitter frequency. In this respect it is similar to amplitude modulation.

The level of the jitter sideband relative to the signal, in dB, is given by:

$$R_j = 20\log(J\omega_i/4) \quad \text{dB} \tag{1}$$

For sinusoidal jitter of amplitude J = 500ps, a 20kHz maximum level tone will produce sidebands at -96.1 dB relative to the input tone.

These results agree with those from simulations by Harris [8].

3.3 The audibility of sampling jitter

In an earlier paper [9] the author derived a graph of maximum inaudible jitter amplitude against jitter frequency for worst case sinusoidal signal input. This is reproduced with minor modifications in figure 9.

This shows that for low jitter frequencies the jitter amplitude may be very large before the sidebands become audible, because the sidebands will be close enough to the original signal to be strongly masked. As the jitter frequency rises above 200 Hz our sensitivity to the modulation increases rapidly. This happens because for low signal frequencies the sidebands are no longer masked, though for higher signal frequencies they still fall below the threshold. For jitter frequencies above 1 kHz the signal frequency that can cause unmasked sidebands increases. As sideband level is proportional to signal frequency this results in increasing sensitivity with increasing jitter frequency. This effect produces a slope of - 6dB per octave on the graph. The intercept level of this final slope is determined by the non-masked threshold of hearing relative to the signal level. The figure was drawn for a playback level of no more than 120dB SPL, assuming the worst case of sidebands being audible at 0dB SPL.

This plot can be used as a specification for allowable sampling jitter in Nyquist sampled systems. At 20 kHz the peak to peak sampling jitter must be less than 20 ps, increasing at 6dB per octave for lower frequencies until approximately 500 Hz where the limit is 1 ns. Below 200 Hz the jitter may up to 500 ns in amplitude before the sidebands could become audible.

For oversampled systems the sampling jitter sensitivity may be worse. As the sampled signal could have a higher frequency than the Nyquist worst case figure of 24 kHz the sensitivity increases further. For a delta-sigma DAC any jitter at 150 kHz, for example, may modulate with the shaped modulator noise at around that frequency creating modulation products falling in the most critical parts of the audio spectrum.

3.4 Sampling jitter measurement techniques

The effect of audio frequency sampling jitter is most clear with a high audio frequency tone being modulated - as this produces modulation products that stand out above the noise floor most clearly.

Jitter sensitivity can be measured by applying signals that introduce known jitter, such as those described in the section on interface jitter. The spectrum of the final result can be inspected for sidebands. Figure 10 shows such a test arrangement for a DAC. An ADC will obviously require an analogue input in addition to the synchronisation source, and a sample rate convertor requires a second digital input in addition to the synchronisation source.

Figure 11 shows the results from such a test. A 20kHz digitally generated tone was modulated by approximately 20ns peak to peak jitter at 17 kHz. The sideband produced is at -65 dB with respect the to 20kHz signal. (On the display the function panel shows the ratio of tone to total distortion and noise products and the level panel indicates the digital level at the measurement ADC)

Applying the formula (1) predicts jitter sidebands at -64 dB. The difference between the two figures is not significant enough to indicate any jitter attenuation occurring at 17 kHz.

(The distortion component at 8kHz on these plots is the aliased 2nd harmonic of the signal tone. This is occurring in the ADC used for this test. This is within a consumer DAT machine, with the signal level driving it boosted in the analogue domain to reduce the significance of the errors it produces)

Figure 12 shows the jitter sidebands produced by another DAC (DAC2a) when driven by an 11 kHz tone at -20 dBFS. The digital input is modulated by about 20 ns of jitter at 5kHz. This shows both sidebands. The indicated distortion level of -67.5 dB (for the two sidebands combined) implies a

sampling jitter amplitude of 17.3 ns. This result indicates that there is no significant attenuation of jitter before the sampling point in this unit at 5 kHz.

The next figure (13) shows the same DAC but with a better PLL circuit being selected (DAC2b). This has attenuated the jitter sidebands at 6 and 16 kHz by at least 30dB so that they are no longer visible. This indicates that the sampling jitter is now less than 600ps at 5kHz.

The following results were taken from DAC2a/b, feeding it from various sources without using the jitter modulator. Any jitter products shown are being induced by the line as described in section 2.3.

Figure 14 shows the output of the DAC with poorer PLL circuit (DAC2a) being driven by 11 kHz at maximum level (0dBFS) on the A channel, and by 2kHz at -80dB on the B channel. The output of the A channel is shown. In addition to the second harmonic distortion in the ADC at 22kHz there are discrete jitter sidebands at 9kHz, 13kHz and 17kHz. (The broad side lobes at 10 and 12 kHz show other wider bandwidth jitter also present at 1 kHz) The low level signal in the B channel is adding jitter at its 1st and 3rd harmonic frequency. This is strongly tonal because, being at low level, most of the data bits are being modulated together - following the two's complement sign bit. Increasing the level in that channel reduces the amplitude of these components. This is shown in figure 15.

All the previous plots were made using the electrical coaxial input to the unit. The optical input has different characteristics as shown in the following:

Figure 16 shows the same test as was on the coaxial input for figure 14. It shows a higher noise floor above 5 kHz and more sidebands- including an even harmonic of the 2 kHz square wave jitter at 3 and 19 kHz. The increased level of the high order harmonics may be significant.

Figure 17 shows the effect of switching to the better PLL on this unit. None of the jitter sidebands is visible in any of the tests using this setting. Also notice how the noise floor is reduced to the level it has with the electrical input. This indicates that the optical input may be producing high bandwidth jitter that is modulating high frequency noise back into the audio band. Note that the device used in this unit is not the Crystal CS4328, which has a `sample domain' switched-capacitor filter to attenuate delta-sigma modulation noise before this re-sampling occurs [10].

4. CONCLUSION

Digital audio equipment has to be designed to cope with jitter from its synchronisation source, as this is a characteristic of the interface. This is particularly important for the recovery of sampling clocks from interface signals.

The assessment of sampling jitter sensitivity can use audio test equipment and does not require examination of signals internal to the unit. Several consumer DAC units have been examined - only one of which behaves in an appropriate manner when fed by a digital signal with jitter.

5. REFERENCES

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FIGURES

1. Simple high frequency loss model for data link.
2. Simulating the effect of high frequency loss on an AES-3 signal.
3. Simulation results showing the effect of data link time constant, τ, on mid-time slot transition timing variations.
4. Simulation results showing the effect of data link time constant, τ, on end-time slot transition timing variations.
5. Simulation results showing the effect of data link time constant, τ, on transition timing variations on the penultimate transition of preamble Y.
6. Calculated results showing the effect of data link bandwidth on peak to peak transition jitter at the penultimate transition of the Y preamble, and the time slot boundary transitions relative to an ideal jitter free clock.
7. Interface jitter amplitude measurement
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9. Maximum sinusoidal sampling jitter amplitudes that will not produce audible modulation products.
10. Block diagram of sampling jitter sensitivity test for a DAC
11. Fourier transform showing jitter sensitivity of DAC 1 using a 20 kHz probe tone at -20 dBFS with 17 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
12. Fourier transform showing jitter sensitivity of DAC 2a on a 11 kHz probe tone at -20 dBFS with 5 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
13. Fourier transform showing jitter sensitivity of DAC 2b on a 11 kHz probe tone at -20 dBFS with 5 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
14. Fourier transform showing line induced jitter sensitivity of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz, -80 dBFS tone on channel B (Coaxial input used).
15. Fourier transform showing reduced jitter of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz tone on channel B increased to -20dB (Coaxial input used).
16. Fourier transform showing line induced jitter sensitivity of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz, -80 dBFS tone on channel B (Optical input used).
17. Fourier transform showing removal of jitter induced noise with DAC 2b as a result of using the better PLL (with a 11 kHz tone at 0 dBFS on ch. A and 2 kHz at -80dB on ch. B)..
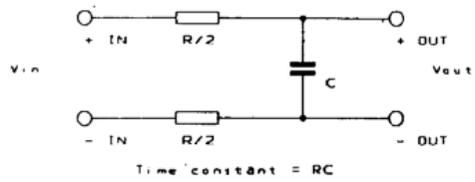
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Figure 1: Simple high frequency loss model for data link.
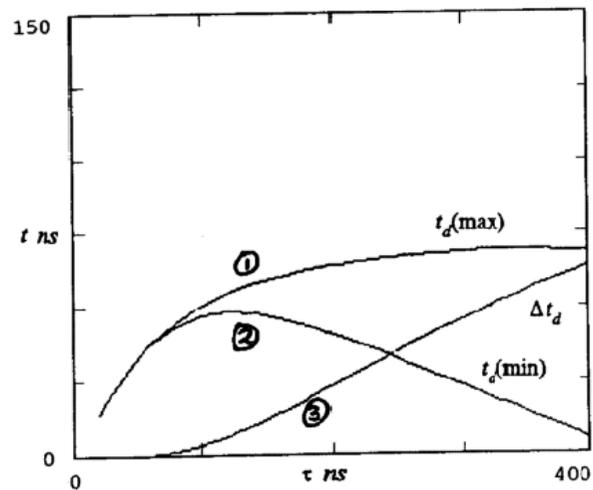
Figure 2: Simulating the effect of high frequency loss on an AES-3 signal.

(Bi-phase data)   (Preamble Y)

Two AES-3 data patterns superimposed

200 ns

50 ns
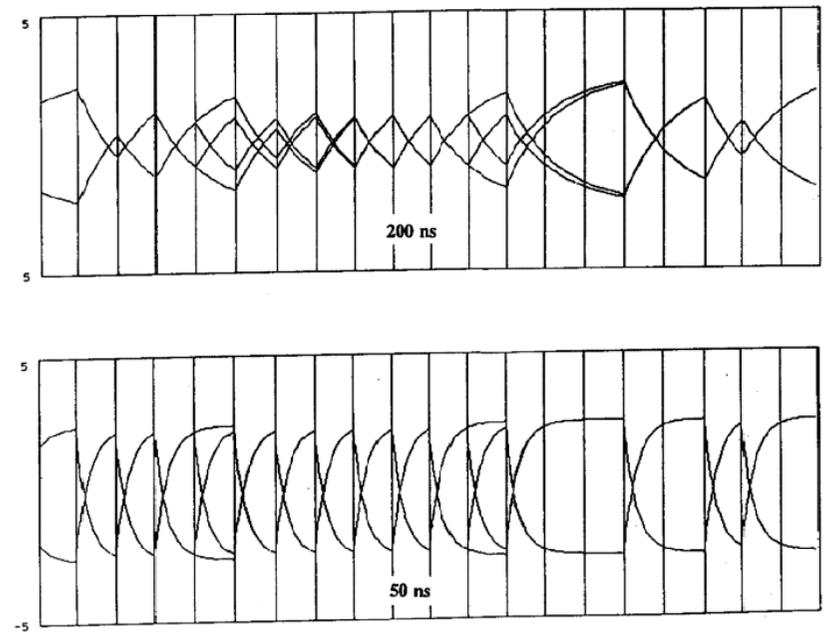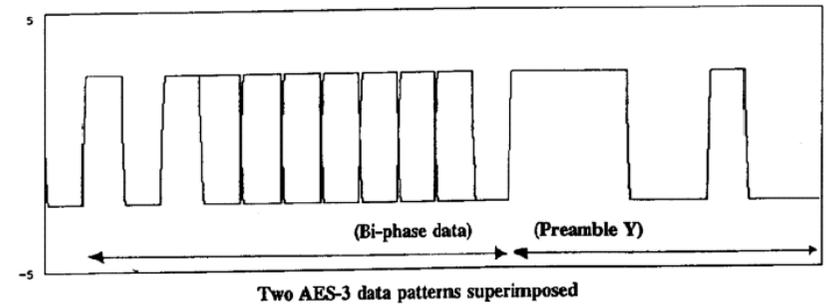
The effect of a low pass network to simulate an interconnection
(both polarities shown for clarity)

Figure 3: Simulation results showing the effect of data link time constant, τ, on mid-time slot transition timing variations.
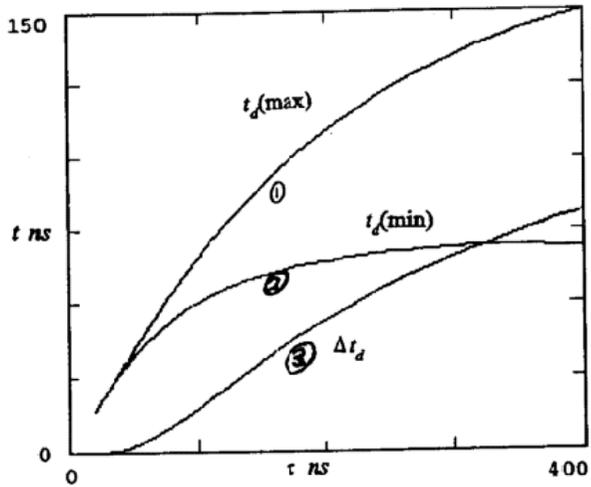
Figure 4: Simulation results showing the effect of data link time constant, τ, on end-time slot transition timing variations.
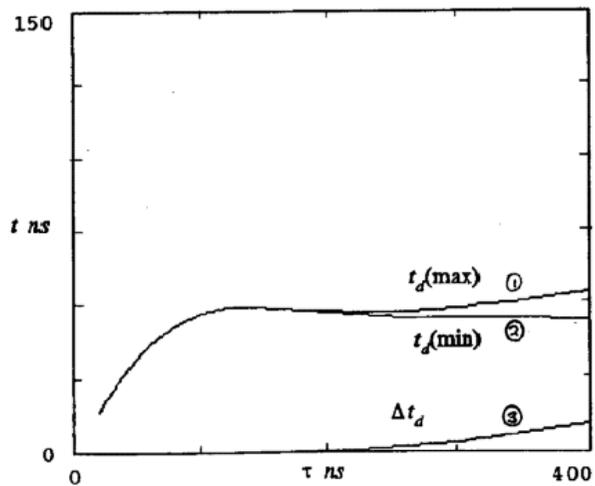
Figure 5: Simulation results showing the effect of data link time constant, τ, on transition timing variations on the penultimate transition of preamble Y.
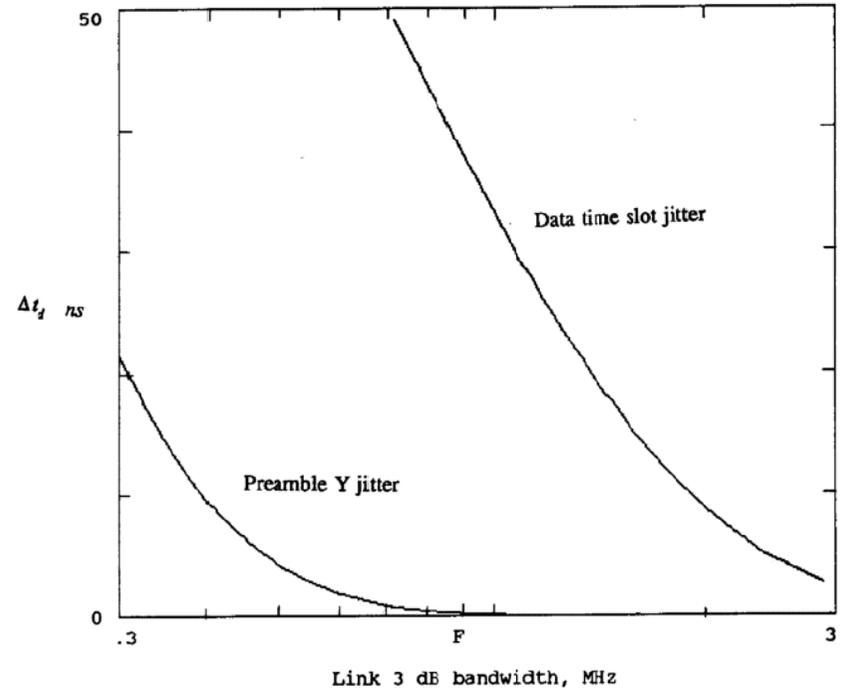
Figure 6: Calculated results showing the effect of data link bandwidth on peak to peak transition jitter at the penultimate transition of the Y preamble, and the time slot boundary transitions relative to an ideal jitter free clock.
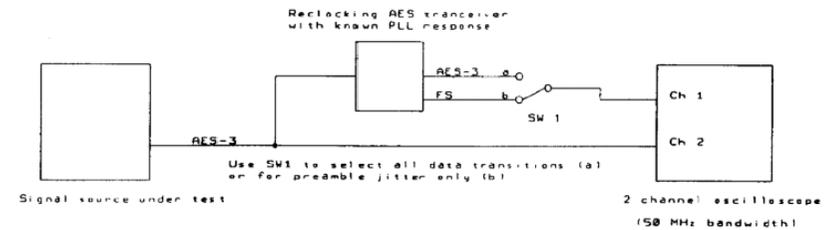
Figure 7: Interface jitter amplitude measurement
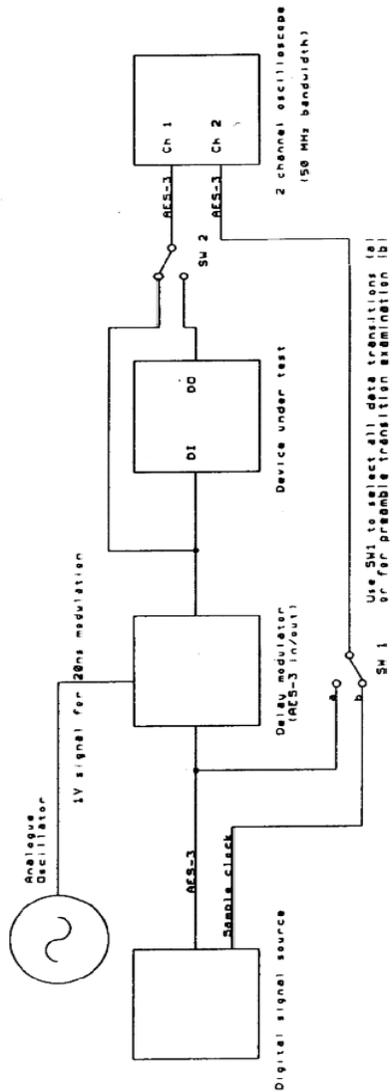
Figure 8: Interface jitter transfer function test arrangement

Maximum inaudible jitter amplitude, J, against frequency, ωⱼ
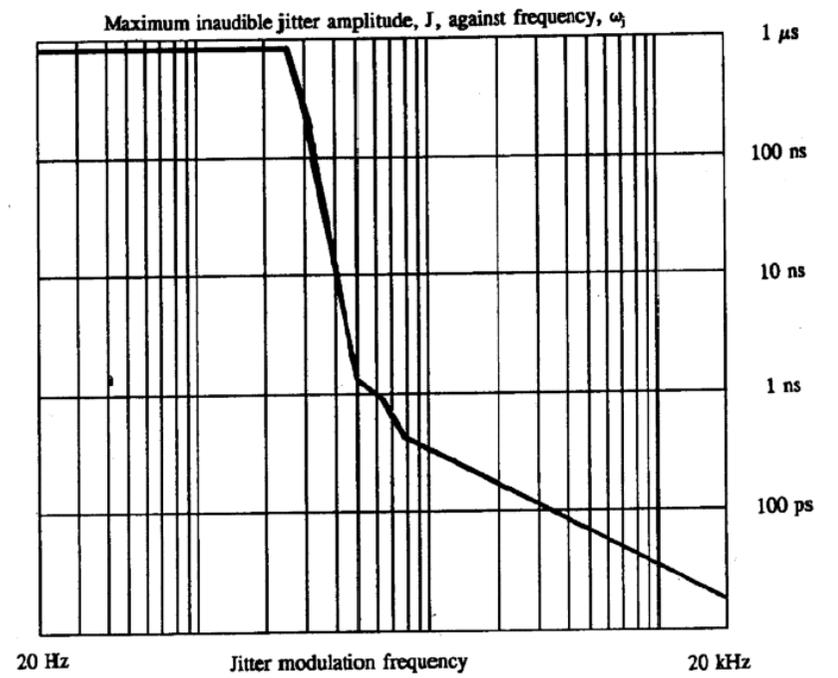
Figure 9: Maximum sinusoidal sampling jitter amplitudes that will not produce audible modulation products.

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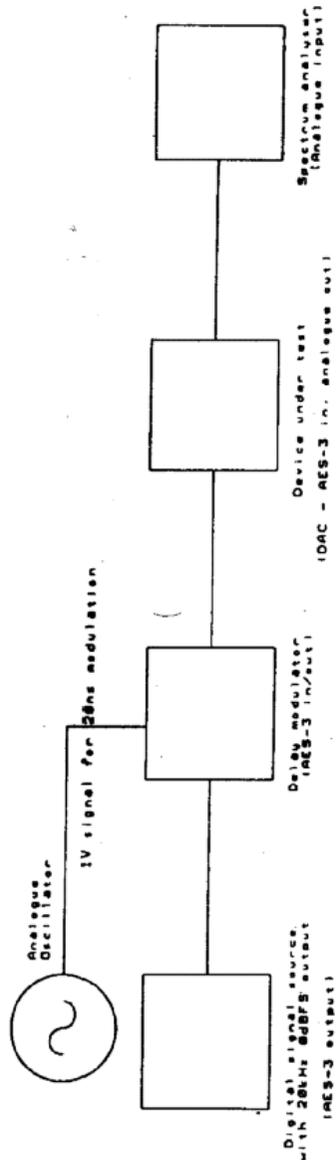
Figure 10: Block diagram of sampling jitter sensitivity test for a DAC
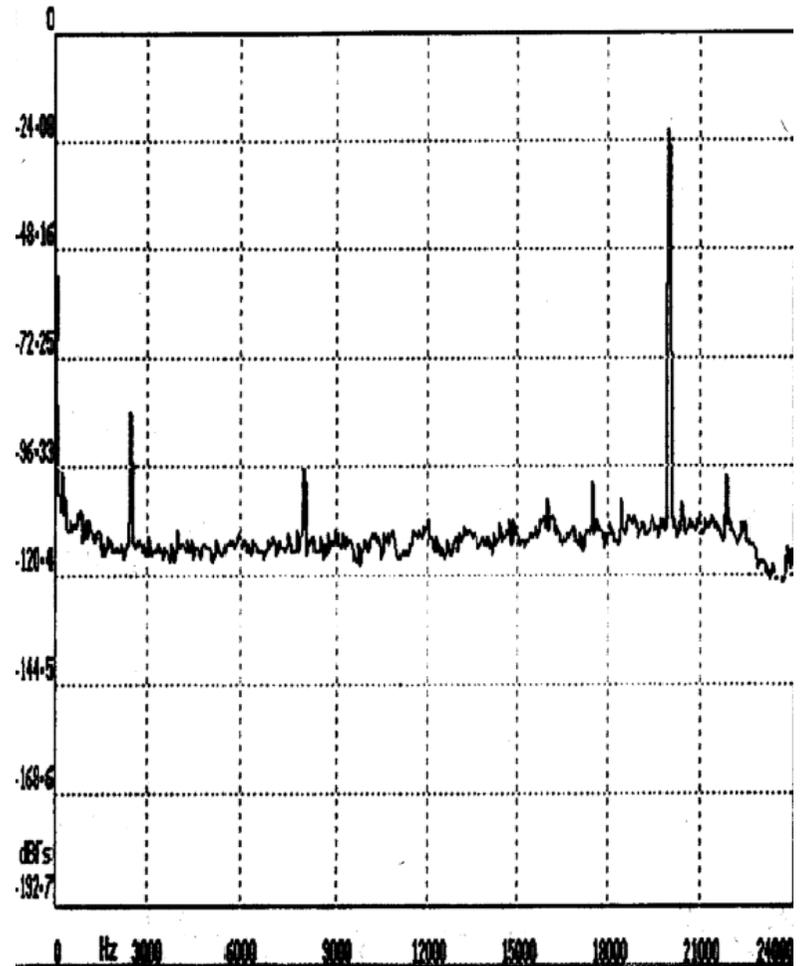
Figure 11: Fourier transform showing jitter sensitivity of DAC 1 using a 20 kHz probe tone at -20 dBFS with 17 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
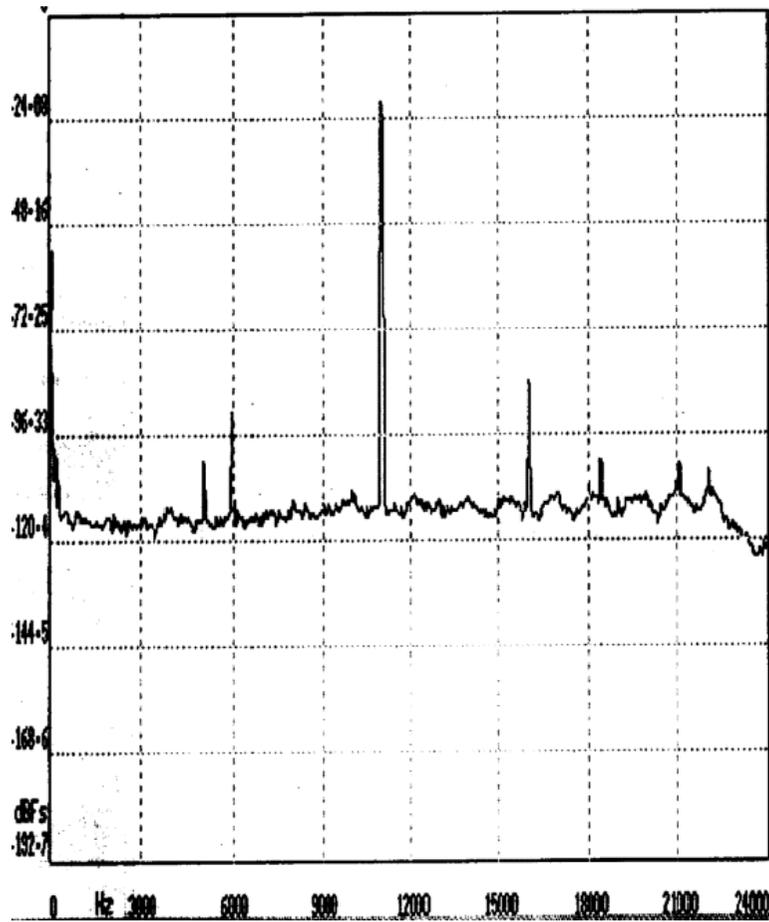
Figure 12: Fourier transform showing jitter sensitivity of DAC 2a on a 11 kHz probe tone at -20 dBFS with 5 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
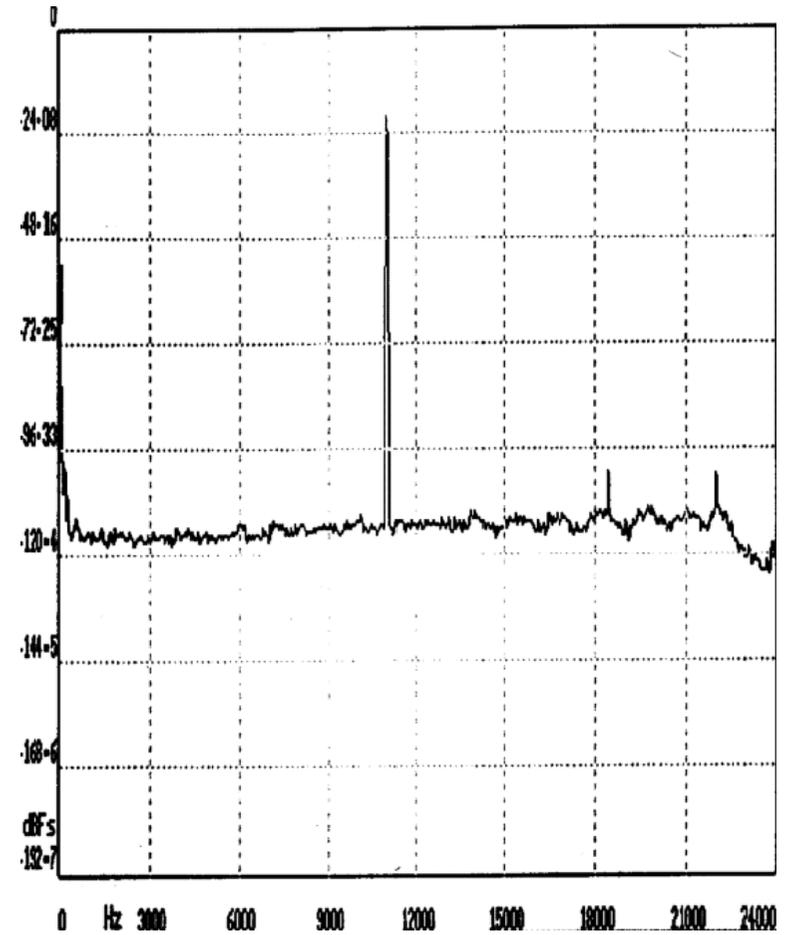

Figure 13: Fourier transform showing jitter sensitivity of DAC 2b on a 11 kHz probe tone at -20 dBFS with 5 kHz sinusoidal jitter at 20ns pk-pk at the digital audio input.
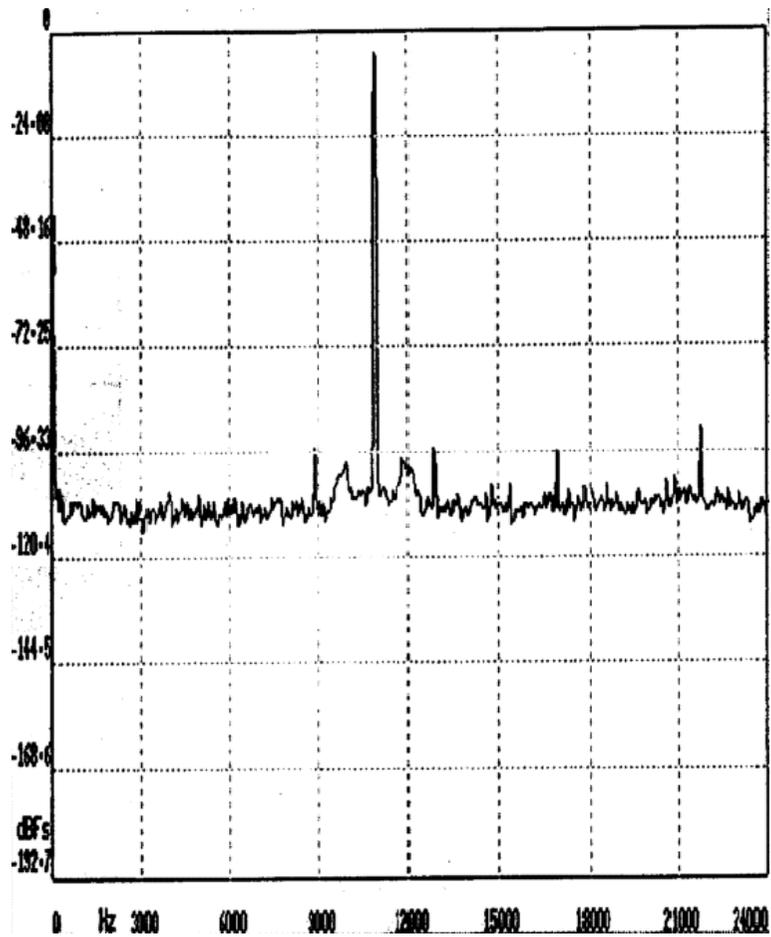
Figure 14: Fourier transform showing line induced jitter sensitivity of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz, -80 dBFS tone on channel B (Coaxial input used).
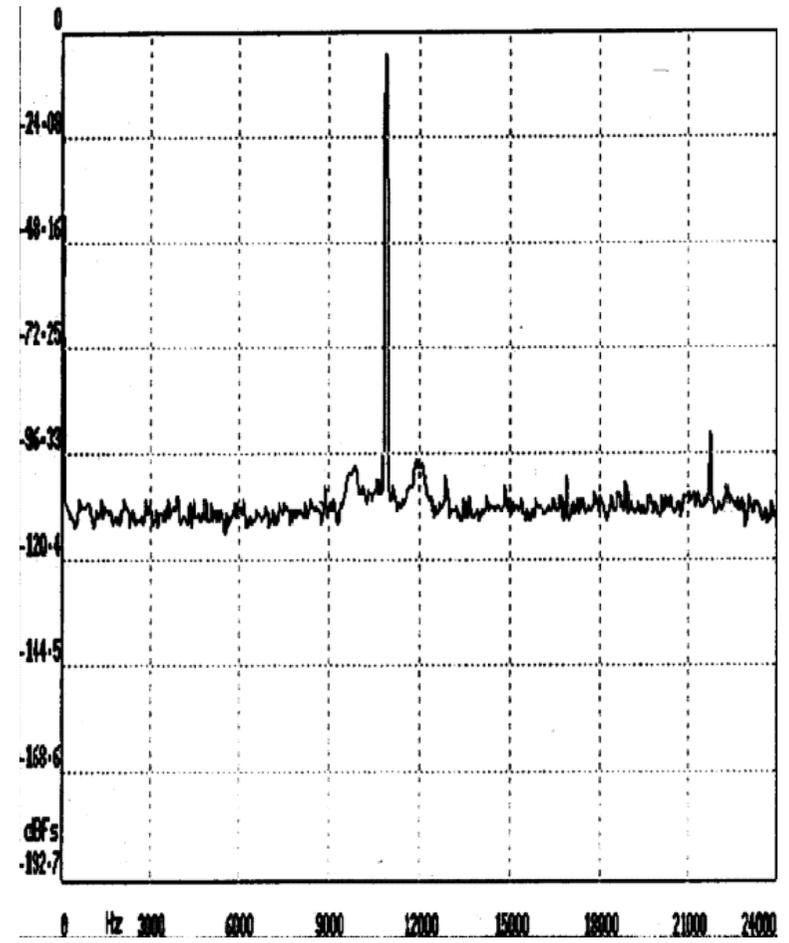

Figure 15: Fourier transform showing reduced jitter of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz tone on channel B increased to -20dB (Coaxial input used).
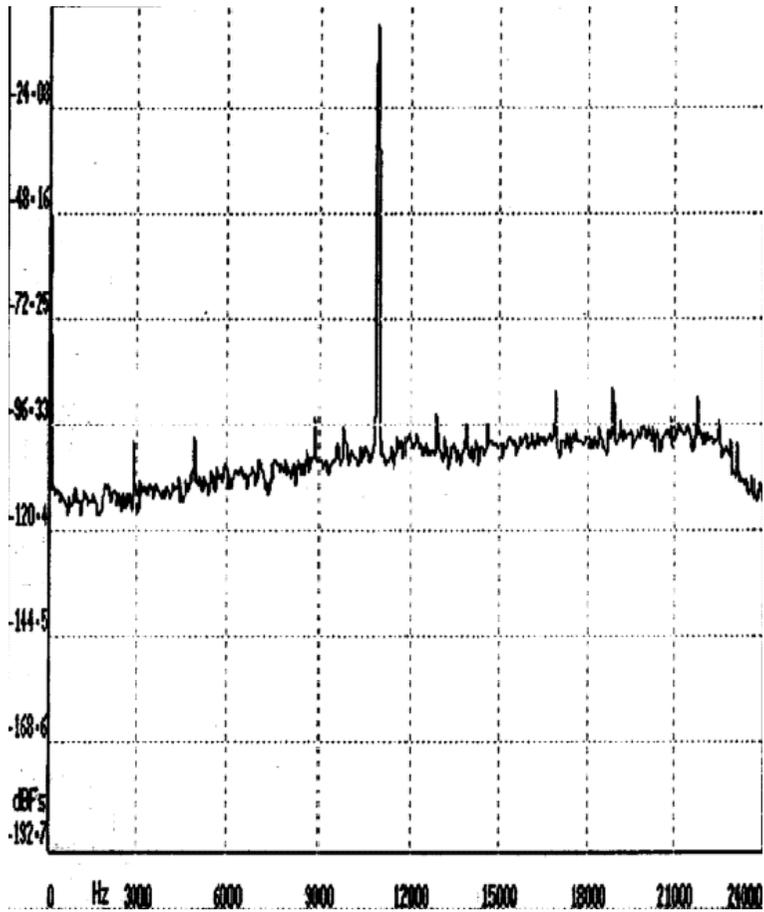
Figure 16: Fourier transform showing line induced jitter sensitivity of DAC 2a with a 11 kHz tone at 0 dBFS on channel A with 2 kHz, -80 dBFS tone on channel B (Optical input used).
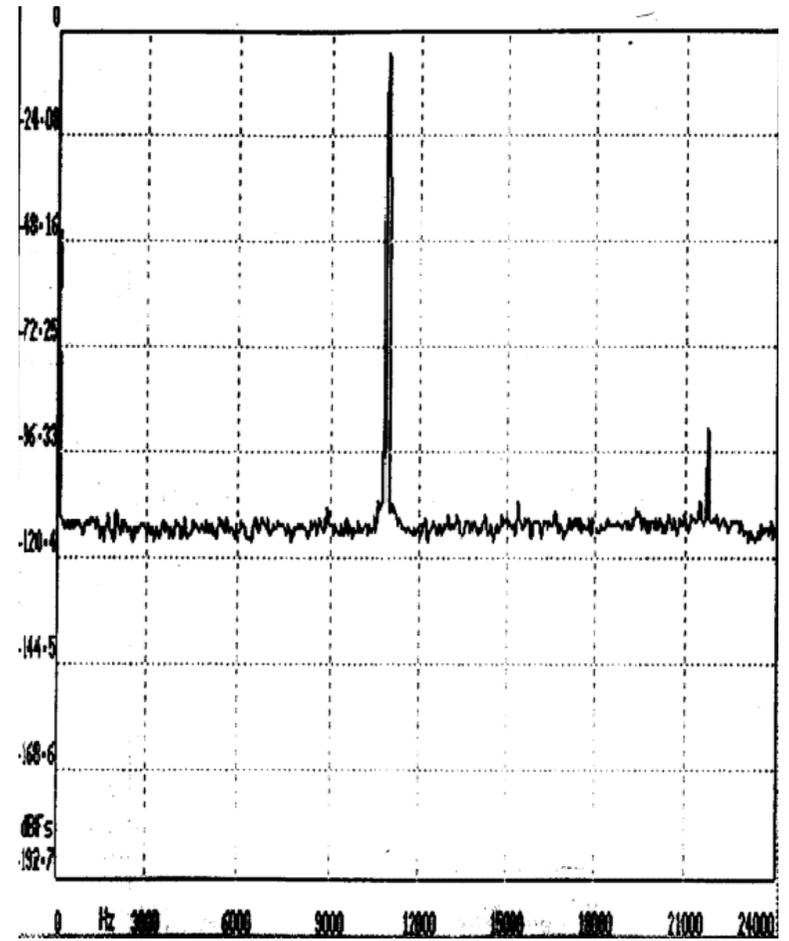

Figure 17: Fourier transform showing removal of jitter induced noise with DAC 2b as a result of using the better PLL (with a 11 kHz tone at 0 dBFS on ch. A and 2 kHz at -80dB on ch. B